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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/814,714	03/23/2001	Satoshi Kamiya	017446/0310	4370

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EXAMINER	
RYMAN, DANIEL J	

ART UNIT	PAPER NUMBER
2665	

DATE MAILED: 02/06/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/814,714	KAMIYA, SATOSHI	
	Examiner	Art Unit	
	Daniel J. Ryman	2665	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *12 December 2005*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-7* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-7* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Arguments

1. Examiner acknowledges Applicant's filing of an RCE on 12/12/2005.

2. Applicant's arguments with respect to claims 1, 2, 3, 5, and 6 have been considered but are moot in view of the new ground(s) of rejection.

3. On page 5 of the Response filed 11/21/2005 and entered on 12/12/2005, Applicant asserts with respect to claim 4 that AAPA and Chao do not suggest performing (1) information transfer processing and (2) reservation processing in a pipeline fashion. Examiner, respectfully, disagrees. Examiner maintains that AAPA in combination with Chao suggests performing pipeline processing in a scheduler (Chao: col. 6, lines 27-37) where the scheduler performs (1) information transfer processing and (2) reservation processing (AAPA: Figs. 8, 9, and 13 and page 1, line 14-page 10, line 14), as outlined in the rejection below.

4. On page 6 of the Response, Applicant asserts that Hanaki "does not disclose or suggest that information transfer processing and reservation processing in a switching system be performed in time slots of the same size such that each of the time slots can only be used for information transfer processing or reservation processing but not for both." Examiner maintains that Hanaki discloses that processing for each stage in a pipeline processor must occur in time slots of the same size (Fig. 2 and col. 1, lines 42-67), as outlined in the rejection below.

5. In addition, Examiner submits that in view of the aforementioned references, it would have been obvious to one of ordinary skill in the art at the time of the invention to use each of the time slots only for information transfer processing or reservation processing but not for both. AAPA's Fig. 13 outlines the sequence of processes that would be broken into various stages to

implement a pipeline processor. The sequence of processes in Fig. 13 would logically be broken in either of two ways: (1) using four stages which include: stage 1 for information transfer (reception) (T0-T1); stage 2 for information expansion (T1-T2); stage 3 for reservation processing (T2-T3); and stage 4 for format conversion (T3-T4) or (2) using three stages which include: stage 1 for information transfer (reception) and information expansion (T0-T2); stage 2 for reservation processing (T2-T3); and stage 3 for format conversion (T3-T4). These divisions for the stages separate out each of the distinct processes of Fig. 13 into separate stages (first processor configuration) or separate out groupings of the distinct processes into stages that require substantially equal time to complete (second processor configuration). In either case, each stage performs either information transfer processing (which, as broadly defined, includes the information transfer process, the information expansion process, and the format conversion process) or reservation processing, but not both. As such, Examiner submits that it would have been obvious to one of ordinary skill in the art at the time of the invention to have each stage use a particular time slot only for information transfer processing or reservation processing but not for both.

6. In view of the foregoing arguments, Examiner maintains that the limitations of claims 4 and 7 are obvious in view of the cited prior art.

Claim Rejections - 35 USC § 112

7. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

8. Claims 1, 2, 3, 5, and 6 are rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

9. Claim 1 discloses that the scheduler "independently assign[s] times slots . . . to information transfer processing and reservation processing, respectively". Thus, a single time slot can be assigned to either information transfer processing or reservation processing by the scheduler, such that each time slot is capable of being used for either information transfer processing or reservation processing prior to assignment by the scheduler. However, claim 1 further discloses that "each of the time slots can only be used for either information transfer processing or reservation processing but not for both information transfer processing and reservation processing". Thus, the claim requires that an individual time slot can be independently assigned to information transfer processing or reservation processing but also be used for either, but not both information transfer processing and reservation processing. Simply, if a particular slot is dedicated to information transfer processing such that it cannot be used for reservation processing, then the scheduler can not "independently assign" the slot to either information transfer processing or reservation processing. Since Examiner is unsure of the metes and bounds of the claim, Examiner will not examiner the claim with respect to the prior art; rather, Examiner will rely on the prior art rejection of claim 4 to indicate to Applicant the state of the prior art.

10. Claim 3, line 7, discloses that the scheduler "perform[s] reservation processing for different time slots". Claim 3, lines 13 and 14, disclose "wherein each of the time slots can only be used for either information transfer processing or reservation processing but not for both

information transfer processing and reservation processing". Thus, the claim requires that the reservation processing both be performed *for* a time slot and *in* a time slot. Examiner suggests that Applicant distinguish between "reservation time slots," which are the time slots corresponding to the reservation process in the pipeline processor, and "packet transferring time slots," which are the time slots that are being reserved in the switch by the use of the pipeline processor. Since Examiner is unsure of the metes and bounds of the claim, Examiner will not examiner the claim with respect to the prior art; rather, Examiner will rely on the prior art rejection of claim 4 to indicate to Applicant the state of the prior art.

Claim Rejections - 35 USC § 103

11. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

12. Claims 4 and 7 are rejected under 35 U.S.C. 103(a) as being unpatentable over Applicant's Admitted Prior Art (AAPA) in view of Chao et al. (USPN 5,724,351), of record, in further view of Hanaki (USPN 6,269,439), of record.

13. Regarding claim 4, Applicant admits as prior art a distributed scheduler for distributed pipeline scheduling which is used by a packet switch in a packet switching system (Fig. 8 and page 1, line 14-page 4, line 21), comprising: a plurality of input modules respectively having output port reservation information receiving sections, allocators, and output port reservation information transmitting sections and serving to perform distributed scheduling (Figs. 8, 9, and 13 and page 1, line 14-page 10, line 14), wherein said output port reservation information

receiving sections, allocators, and output port reservation information transmitting sections execute processing for different reservation time slots (Figs. 8, 9, and 13; page 1, line 14-page 5, line 24; and page 8, line 17-page 10, line 14).

Applicant does not admit as prior art that the output port reservation information receiving sections, allocators, and output port reservation information transmitting sections within each input module simultaneously execute processing for different reservation time slots, i.e. implementing pipeline processing within each input module. Chao teaches, in a packet switching system, that adequate performance of a large switch is only possible by using pipeline techniques in the scheduler (arbiter) (col. 6, lines 27-37); however, Chao does not specify how the pipeline processing is performed. Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to perform pipeline processing in each input module in order to have adequate performance in a large switch.

Applicant in view of Chao does not expressly disclose the output port reservation information receiving sections, allocators, and output port reservation information transmitting sections within each input module simultaneously execute processing for different reservation time slots wherein the processing comprises information transfer processing and reservation processing performed, respectively, in time slots of the same size and wherein each of the time slots can only be used for either information transfer processing or reservation processing but not for both information transfer processing and reservation processing. However, Applicant admits as prior art that the processing comprises distinct processes such as information transfer processing (which, as broadly defined, includes the information transfer process, the information expansion process, and the format conversion process) and reservation processing (Fig. 13 and

page 8, line 19-page 9, line 15). Chao teaches using pipeline processing in a scheduler (col. 6, lines 27-37). Hanaki teaches, in a pipeline processing system, simultaneously executing processing for different items in the elements of a pipeline processor in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing, wherein the processing comprises processing of each stage in time slots of the same size (time for IF cycle is the same as for the ID cycle, EX cycle, etc.) (Fig. 2 and col. 1, lines 42-67). Thus, it would have been obvious to one of ordinary skill in the art at the time of the invention to have the output port reservation information receiving sections, allocators, and output port reservation information transmitting sections within each input module simultaneously execute processing for different reservation time slots, wherein the processing comprises information transfer processing and reservation processing performed, respectively, in time slots of the same size, in order to increase the amount of processing that can be accomplished per unit time compared to a processor without pipeline processing.

In addition, it would have been obvious to one of ordinary skill in the art at the time of the invention to break the processing performed by the input module among the stages of a pipeline processor into input information transfer processing, reservation processing, and output information transfer processing (see Applicant's Fig. 13) in order to implement the pipeline processor, such that each of the time slots can only be used for either information transfer processing or reservation processing but not for both information transfer processing and reservation processing. AAPA's Fig. 13 outlines the sequence of processes that would be broken into various stages to implement a pipeline processor. The sequence of processes in Fig. 13 would logically be broken in either of two ways: (1) using four stages which include: stage 1 for

information transfer (reception) (T0-T1); stage 2 for information expansion (T1-T2); stage 3 for reservation processing (T2-T3); and stage 4 for format conversion (T3-T4) or (2) using three stages which include: stage 1 for information transfer (reception) and information expansion (T0-T2); stage 2 for reservation processing (T2-T3); and stage 3 for format conversion (T3-T4). These divisions for the stages separate out each of the distinct processes of Fig. 13 into separate stages (first processor configuration) or separate out groupings of the distinct processes into stages that require substantially equal time to complete (second processor configuration). In either case, each stage performs either information transfer processing (which, as broadly defined, includes the information transfer process, the information expansion process, and the format conversion process) or reservation processing, but not both. As such, it would have been obvious to one of ordinary skill in the art at the time of the invention to break the processing performed by the input module among the stages of a pipeline processor into input information transfer processing, reservation processing, and output information transfer processing in order to implement the pipeline processor, such that each of the time slots can only be used for either information transfer processing or reservation processing but not for both information transfer processing and reservation processing

14. Regarding claim 7, Applicant in view of Chao in further view of Hanaki implicitly discloses that the time slots of the same size are determined as being the largest among (a) time for information transfer reception and information expansion, (b) time for reservation processing, and (c) time for format conversion and information transfer transmission (Hanaki: Fig. 2 and col. 1, lines 42-67) where, since one stage cannot pass its processed information to the next stage

until the next stage is completed, the length of the time slot/cycle for each stage to complete processing is determined by the longest processing time required by a stage in a pipeline.

Conclusion

15. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure. Jordan et al. (USPN 5,805,849), of record, see col. 1, lines 52-67 which pertain to the benefits of pipelined processors. Kumar (USPN 6,122,274), of record, see entire document which pertains to a decentralized pipeline control for a switch.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Daniel J. Ryman whose telephone number is (571)272-3152. The examiner can normally be reached on Mon.-Fri. 7:00-4:30 with every other Friday off.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Huy Vu can be reached on (571)272-3155. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DJR

Daniel J. Ryman
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